Best Design and Layout Practices for SiTime Oscillators

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1 Introduction

Proper decoupling, bypassing, and power supply noise reduction is important in many applications to ensure optimal performance for oscillators. A common strategy is to place capacitors near high speed devices on a printed circuit board (PCB). These capacitors serve important functions:

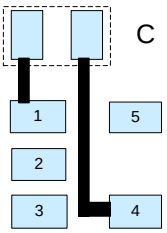
- Provide instantaneous current to the component
- Reduce noise propagation through the system
- Shunt the power supply noise to GND

The following sections describe decoupling, bypassing, noise rejection, and power supply condition recommendations for SiTime's single-ended and differential timing devices.

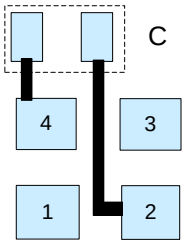
2 Decoupling

Fast switching devices such as clock oscillators can place a significant demand on the power source. The high clock rate coupled with the fast rise time (typically in the 1 ns range) makes it difficult for the power supply to source the required current in a timely manner. As a result, the supply voltage level at the device will sag. To ensure an adequate amount of charge is always available to the device, a decoupling capacitor can be installed to act as a local reservoir.

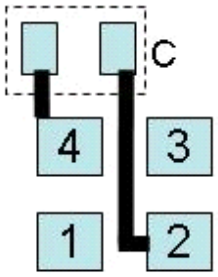
SiTime recommends using a 0.1 µF ceramic decoupling capacitor between the VDD pin of the oscillator and the ground plane for both single-ended and differential devices. Figure 1 and Figure 2 show a sample layout for the SiTime 4-pin oscillator with a 0603-size, 0.1 µF decoupling capacitor C. Figure 3 shows a sample layout of a SiTime chip scale package (CSP). All traces shown in Figures 1, 2 and 3 need to be covered with solder mask. With SiTime's 4-pin devices, pin 1 of the clock may be used to support functions such as output enable, standby, spread disable, VCXO control or auto-calibration. Traces carrying high-edge rate signals and noisy power switched signals should be routed at least 1 mm away and orthogonal to the pin-1 trace. Refer to section 6 for further layout guidelines.



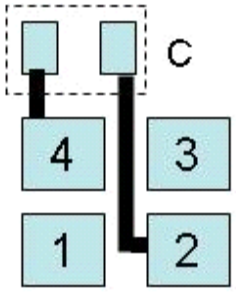
(a) SOT23-5 package



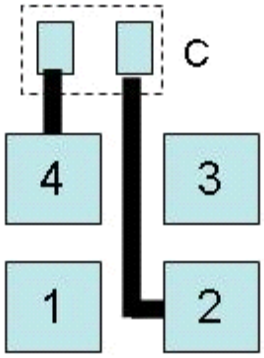
(b) 2.0 mm x 1.6 mm package



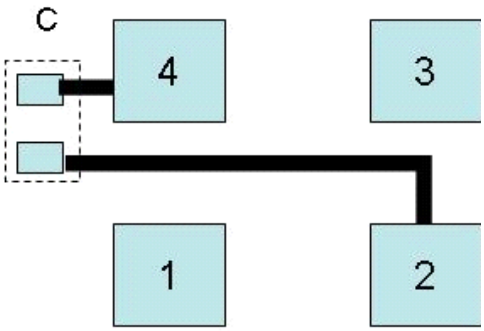
(c) 2.5mm x 2.0mm package



(d) 3.2mm x 2.5mm package

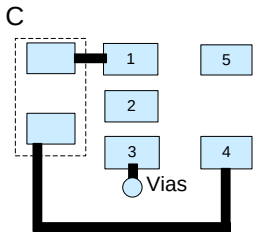


(e) 5.0mm x 3.2mm package

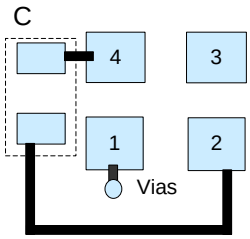


(f) 7.0mm x 5.0mm package

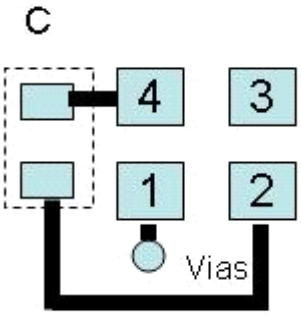
Figure 1: Layout Example of 4-pin SiTime device with a decoupling capacitor when board fabrication allows trace routing between oscillators pins



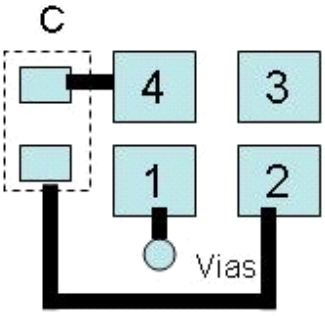
(a) SOT23-5 package



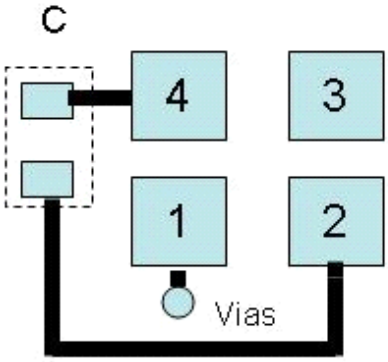
(b) 2.0 mm x 1.6 mm package



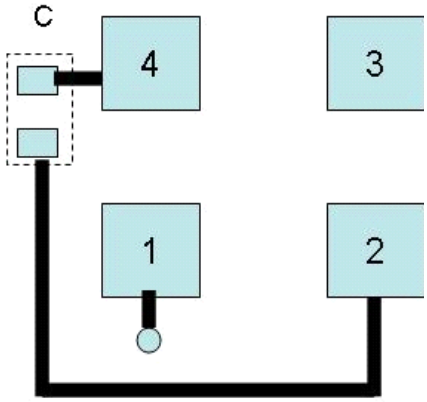
(c) 2.5mm x 2.0mm package



(d) 3.2mm x 2.5mm package

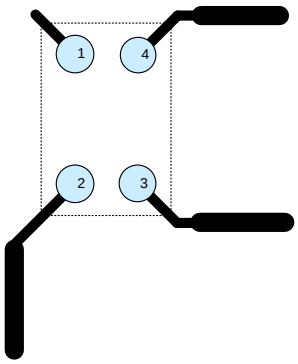


(e) 5.0mm x 3.2mm package



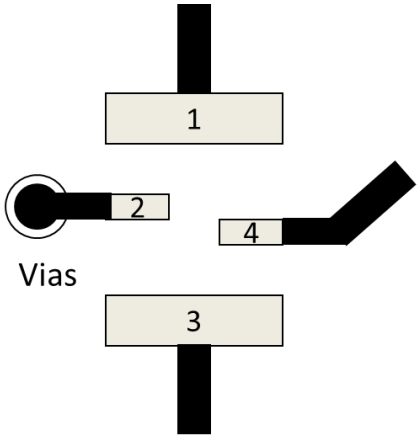
(f) 7.0mm x 5.0mm package

Figure 2: Layout example of a SiTime device with a decoupling capacitor when board production doesn't allow traces between oscillator pins



1.5mm x 0.8mm (CSP) package

Figure 3: Layout example for CSP devices



2.0 mm x 1.2 mm (QFN) package

Figure 4: Layout example for 2012 (QFN) devices

3 Bypassing

With today's high processor speeds and data rates, there is a considerable amount of noise in the system. The nearly square waveforms produced by the clock oscillators contain the fundamental frequency of the unit as well as the higher harmonic components of the signal. To limit the amount of noise propagating through the system, bypass capacitors are needed to provide low-impedance paths to shunt this transient energy to ground.

In most applications, the 0.1 µF decoupling capacitor provides sufficient bypass capability for all SiTime devices. No additional bypass capacitors are required.

The user may consider using an additional 1 nF or 10 nF bypass for SiTime oscillators with differential outputs operating at high frequencies (above 150 MHz) to suppress the higher clock harmonics on the power supply network.

4 Power Supply Noise Reduction

In most applications, a single 0.1 µF capacitor between VDD and GND will shunt much of the noise that may exist on the power supply to GND. SiTime devices use an internal regulator to reduce the impact of the power supply noise. However, to further minimize any residual power supply noise impact on the oscillator output jitter, the user may consider RC or LC power supply filtering strategies. SiTime recommends using such filtering for high-speed applications, such as serial interfaces with greater than 6 Gbps baud rates (e.g., 8.5 Gbps Fibre Channel and Serial 10 Gbit Ethernet).

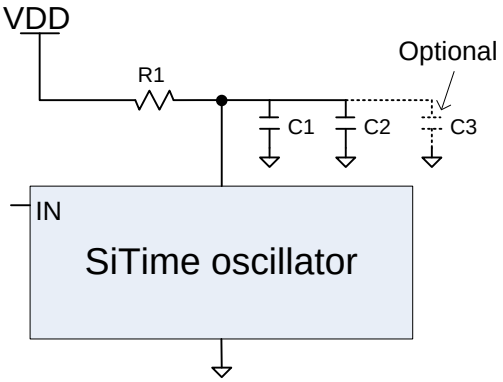


Figure 5: RC power supply filter

The RC filtering, shown in Figure 5, is simple to use. The R needs to be selected such that the nominal voltage drop on the resistor is in the range of 5% of nominal power supply voltage. Table 1 shows the values for different SiTime oscillators.

Table 1: Recommended component values for RC power supply filter

Device	R1 (Ω)	C1 (µF)	C2 (µF)	C3 (µF)
SiT9001, SiT8208, SiT8209, SiT8225, SiT8256, SiT5000, SiT5001, SiT5002, SiT3807, SiT3808, SiT3809, SiT3907	3	10	0.1	0.01
SiT8103, SiT3701, SiT8033, SiT9003, SiT8003, SiT1602, SiT8008, SiT8009, SiT1618, SiT8918, SiT8919, SiT8920, SiT8921, SiT8924, SiT8925, SiT2018, SiT2019, SiT2020, SiT2021, SiT2024, SiT2025, SiT9201, SiT2001, SiT2002, SiT5021, SiT5022	5	1	0.1	N/A

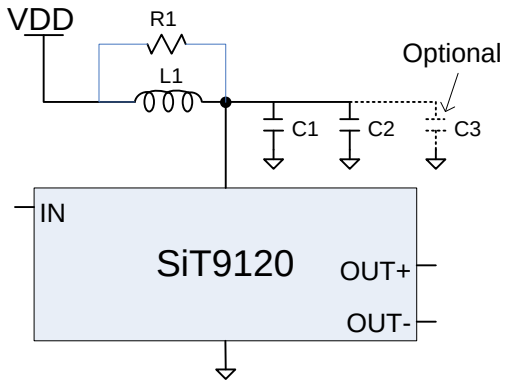


Figure 6: LC power supply filter

LC filtering, shown in Figure 6, is particularly suited for devices with higher current consumption, such as differential oscillators. The inductor low series resistance (typically less than 1Ω) delivers the DC supply voltage to the device with less than 50 mV drop. The LC filter has the added advantage of minimizing potential oscillator switching noise from the power network. The resistor in parallel with inductor is intended to reduce the peaking at the resonance frequency of the LC circuit. Table 2 lists the recommended component values for LC power supply filters for some of the SiTime differential ended devices. The same filter can also be used with other SiTime differential or single-ended oscillators (with and without spread spectrum feature) and VCXO control.

Table 2: Recommended component values for LC power supply filter

Components	L1	C1 (µF)	C2 (µF)	C3 (µF)	R1 (Ω)
SiT9102, SiT9002, SiT9120, SiT9121, SiT9122, SiT9156, SiT3821, SiT3822, SiT3921, SiT3922	1 uH to 10 uH Imax >140 mA	10	0.1	0.01	10

5 Power Supply Management

It is not recommended to power on SiTime oscillators from intermediate electric potential and/or with extreme slow power on ramp rates. Powering on under these conditions may cause the oscillator to malfunction.

6 Layout Recommendations for SiTime Clocks

Following are some common guidelines for PCB layout.

- Use decoupling capacitors between VDD and ground of the clock source are essential to reduce noise that may be transmitted to the clock signal. These capacitors must be places as close to the VDD pin as possible, typically 1 to 2 mm.
- Physically locate the clock source chip as close to the load.
- Limit the trace lengths for clock signals.

- Do not route clock signal close to the board edge.
- Do not route power traces or other high frequency signals below the oscillator PCB area. A ground layer below the oscillator is highly recommended.
- Avoid using vias in clock signal routings if possible. Vias change the trace impedance which may cause reflections.
- Do not route clock traces on the power and ground layer.
- Avoid right angle bends in a trace and if possible keep trace routings straight. If a bend is necessary, use two 45 degree corners or a round bend as shown below.
- When routing differential signals, ensure the electrical length of the traces within the pair match.

6.1 1508 CSP and 2012 QFN Package Layout

Sample PCB layouts for devices in 1508 and 2012 packages are shown in Figures 3 and 4. It is strongly recommended that the PCB designer follow the following layout guidelines.

- Do not connect any of the pads directly to a copper polygon or a wide PCB trace. This may cause bad solder joints due to non-uniform heating transfer during the assembly process.
- Provide short length (1 to 3 mm) and thin width (~0.15 mm) traces to each pad and then to the respective copper polygon or wide trace.
- Keep high current and high speed traces away from the CSP package.
    - Route high-edge rate and noisy signals at least 1 mm away from clock-out and pin-1 signal traces.
    - Use of orthogonal routes is recommended to avoid signal coupling.

Revision History

Version	Release Date	Change Summary
1.0	2/11/11	Original doc
2.0	4/1/12	Document was re-structured.
2.4	12/9/13	Updated with support for 4 pin 2016 packages
2.5	3/17/16	Minor grammatical correction, clarification and added support for 4 pin chip scale(CSP) and 2012 QFN packages

SiTime Corporation
990 Almanor Avenue
Sunnyvale, CA 94085
USA
Phone: 408-328-4400
http://www.sitime.com