Inphi PAM4 Performance when Driving Shared Reference Clocks

Test Case: Using one oscillator vs a multi-output clock generator to drive Inphi PAM4 DSPs

Contents

1 Introduction

The Inphi Polaris and Vega 400G PAM4 DSP families [1] have dual die variants. In some cases, the reference clock (REFCLK) input for each die is brought out separately. In other cases, the reference clocks are connected together on the substrate (in the package) and only one reference clock input is brought out to the device pins.

For all these dual-die variants, it is preferable to use a single REFCLK source to minimize space, cost, and power in the end application.

The Inphi and SiTime applications teams have prepared and tested two reference clock configurations:

1. A SiTime Elite Platform™ SiT9365 156.25 MHz oscillator [2] as a common reference clock for both dies – this is the recommended configuration

2. A quartz clock generator on the Inphi Helios Evaluation Board (EVB) to drive the reference clock inputs of each die individually – this is the default board configuration

The test for both configurations was conducted on the Inphi Helios Evaluation Platform at the Inphi lab. The purpose is to validate that the SiT9365 LVPECL differential clock can simultaneously drive two reference clock inputs of the Inphi PAM4 DSP while achieving optimum performance. All testing was done on the Inphi TX outputs at 28.125 Gbaud with PRBS7 pattern in Line PRBS Mode.

2 Test Setup Overview

The two reference clocks tested are described in Table 1. For comparison purposes, data was collected with a SiT9365-156.25 MHz oscillator as a shared reference clock and the quartz clock generator as the source for the two separate clock inputs of the Inphi PAM4 DSP on the Inphi Helios reference platform.

Table 1: Products tested

Type	z	Number of Clock Outputs Used	Phase Jitter [1] (rms) fs
SiTime SiT9365AI [2]	156.25	1	225
Quartz Clock Generator	156.25	2	115

Note: 1 – Phase jitter integrated over 12 kHz to 20 MHz

The performance parameters measured during the tests are as shown in Table 2.

Table 2: Parameters tested and test conditions

Item	Parameters	Test Setup and Conditions
1a	Eye diagram	Setup-1: SiT9365 driving two reference clock inputs of PAM4 DSP, TX lane differential outputs to Keysight Technologies DCA-X 86100D WB scope (See Figure 2)
1b	BER bath tub, eye width, skew, random Jitter	
2a	Eye diagram	Setup-2: Quartz clock generator two outputs driving reference clock inputs of the PAM4 DSP; TX lane differential outputs to Keysight Technologies DCA-X 86100D WB scope (See Figure 3)
2b	BER bath tub, eye width, skew, random jitter	

The test setup details and conditions are covered in the following sections.

3 Test Setup and Conditions

All testing was done on the Inphi Helios evaluation platform. This platform uses two LVPECL clock outputs of the on-board quartz clock generator to drive the two reference clock inputs of the PAM4 DSP. This is the default board configuration.

Test Setup-1: The Inphi Helios evaluation platform was modified such that the on-board quartz clock generator outputs were bypassed and a SiT9365-LVPECL oscillator output was wired-in to drive both reference clock inputs of the PAM4 DSP. This is shown in Figure 1.

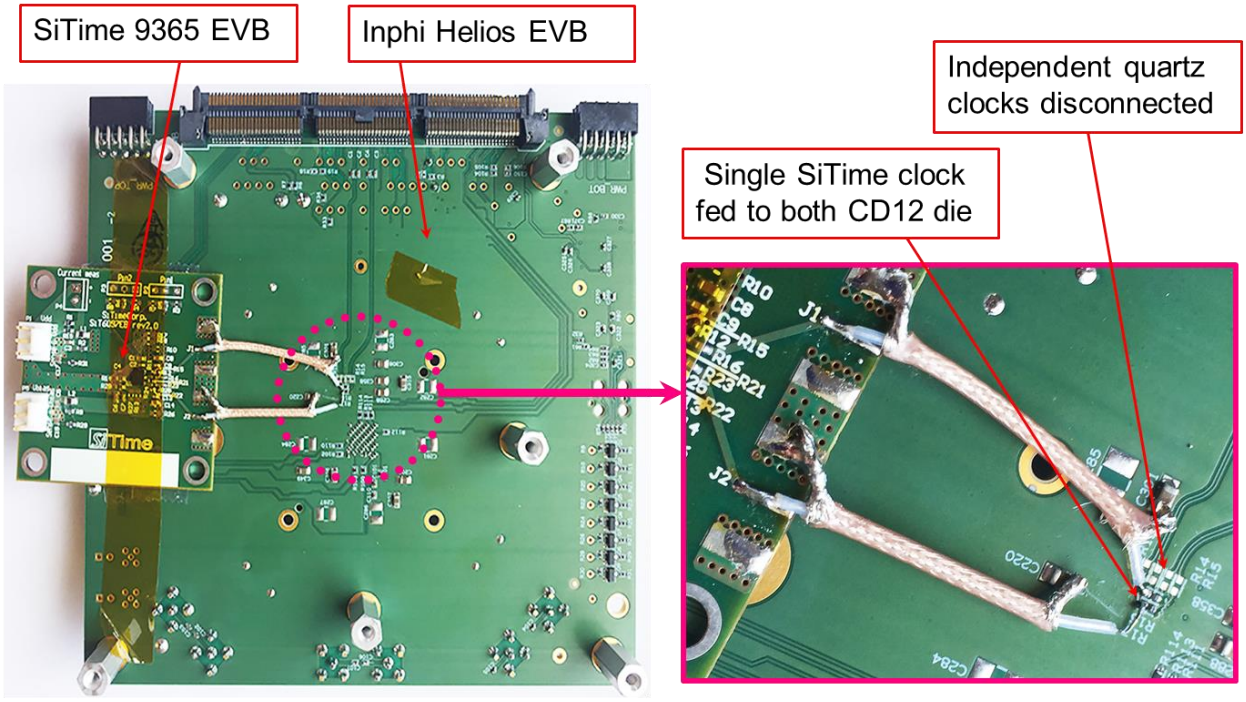


Figure 1: A snippet of the test setup used to bypass the default configuration to drive both reference clock inputs of the Inphi PAM4 DSP with one SiT9365-LVPECL oscillator.

A block diagram of the complete Test Setup-1 is shown in Figure 2.

Test Setup-2: Two LVPECL outputs of the quartz clock generator each driving one of the two reference clock inputs of the PAM4 DSP is shown in the block diagram of Figure 3.

A Keysight Technologies DCA-X 86100D wide bandwidth scope was used to measure eye diagram and jitter related parameters on one of the 28.125 Gbaud PAM4 TX lanes of the Inphi PAM4 DSP.

3.1 Test Setup-1: SiT9365 driving two reference-clock inputs

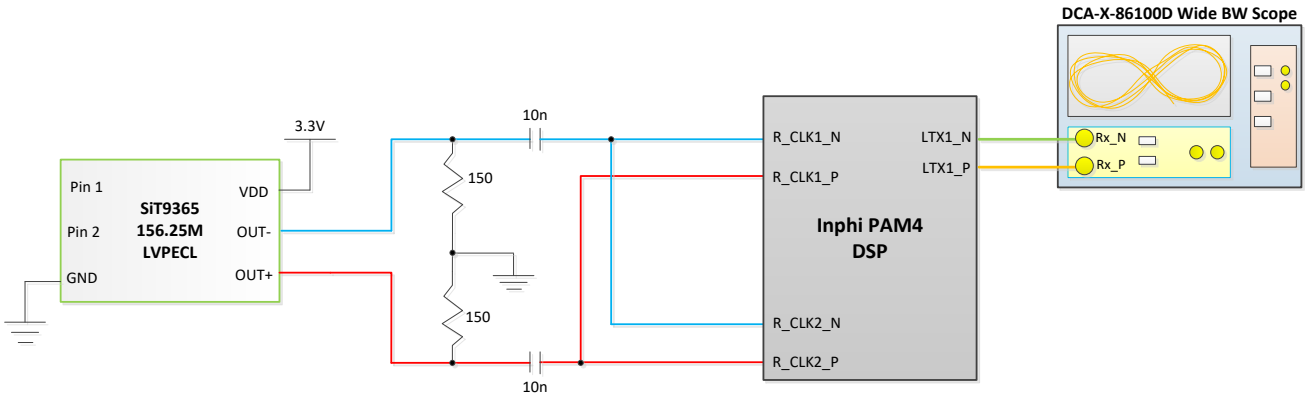


Figure 2: Test setup for measuring eye diagram and jitter on a 28.125 Gbaud TX lane of Inphi PAM4 DSP with both reference-clock inputs driven by a SiT9365-156.25 MHz oscillator.

After connecting one of the 28.125 Gbaud TX lanes to the DCA-X as illustrated in Figure 2, the PAM4 DSP was configured to send the PRBS7 pattern at 28.125 GBaud PAM4. The DCA-X was configured to display the eye diagram and measure the jitter/noise parameters on one of the TX lanes.

3.2 Test Setup-2: Quartz clock generator driving two reference clock inputs

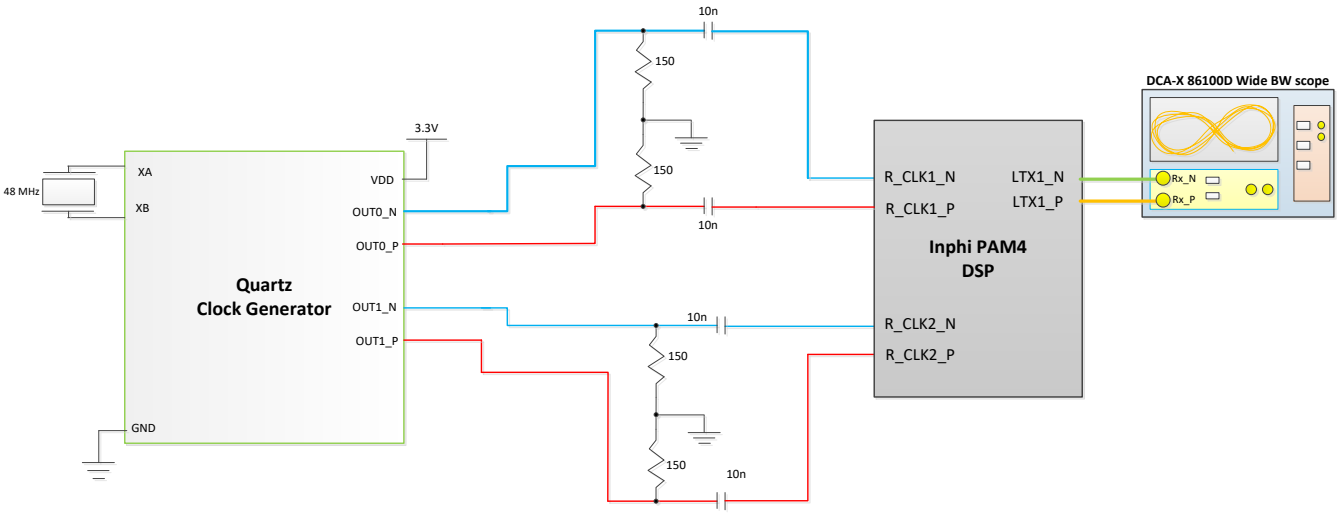


Figure 3: Test setup for measuring eye diagram and jitter on a 28.125 Gbaud TX lane of Inphi CD12 PAM4 PHY with each reference-clock input driven by the quartz clock generator.

After connecting one of the 28.125 Gbaud TX lanes to the DCA-X as illustrated in Figure 3, the PAM4 DSP was configured to send PRBS7 pattern at 28.125 Gbaud PAM4. The DCA-X was configured to display the eye diagram and measure the jitter/noise parameters on one of the data lanes.

4 Measurement Results

4.1 Setup-1: Performance with SiT9365-156.25 MHz oscillator

The eye diagram as measured on the DCA-86100D with the SiT9365 as a shared reference clock is shown in Figure 4.

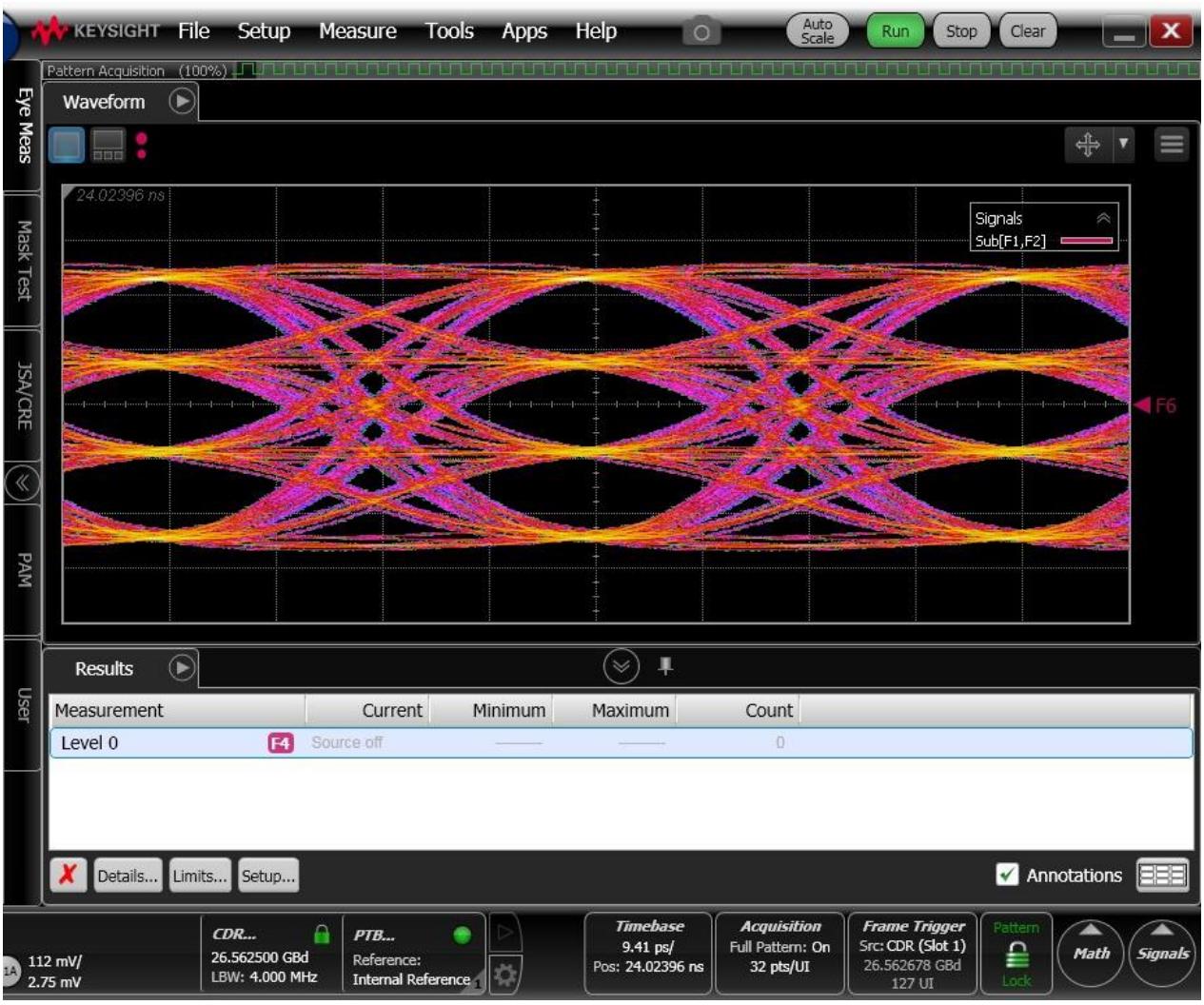
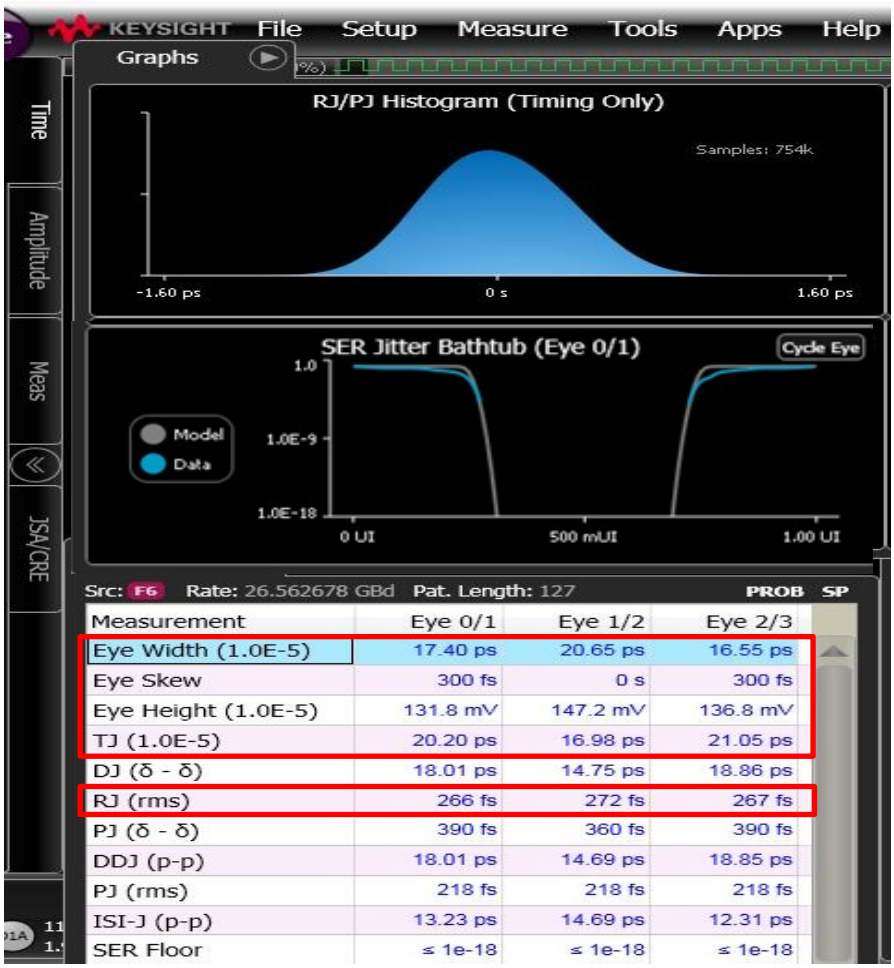


Figure 4: PAM4 DSP TX lane eye diagram with a SiT9365-156.25 MHz clock as a shared reference clock.

The jitter performance parameters for the PAM4 DSP TX lane are shown in Figure 5.



Measurement	Eye 0/1	Eye 1/2	Eye 2/3
Eye Width (1.0E-5)	17.40 ps	20.65 ps	16.55 ps
Eye Skew	300 fs	0 s	300 fs
Eye Height (1.0E-5)	131.8 mV	147.2 mV	136.8 mV
TJ (1.0E-5)	20.20 ps	16.98 ps	21.05 ps
DJ (δ - δ)	18.01 ps	14.75 ps	18.86 ps
RJ (rms)	266 fs	272 fs	267 fs
PJ (δ - δ)	390 fs	360 fs	390 fs
DDJ (p-p)	18.01 ps	14.69 ps	18.85 ps
PJ (rms)	218 fs	218 fs	218 fs
ISI-J (p-p)	13.23 ps	14.69 ps	12.31 ps
SER Floor	≤ 1e-18	≤ 1e-18	≤ 1e-18

Figure 5: PAM4 DSP TX-1 data lane jitter performance parameters with a SiT9365-156.25 MHz clock as a shared reference clock.

Note that the reference clock contribution to the PHY TX lane eye is indicated by the following measured parameters:

1. Eye width
2. Eye skew
3. Eye height
4. SER jitter bathtub
5. Random jitter (RJ)

4.2 Setup-2: Performance with quartz clock generator

The eye diagram as measured on the DCA-86100D with the quartz clock generator driving each of the two reference clock inputs independently (separate clock generator outputs) is shown in Figure 6.

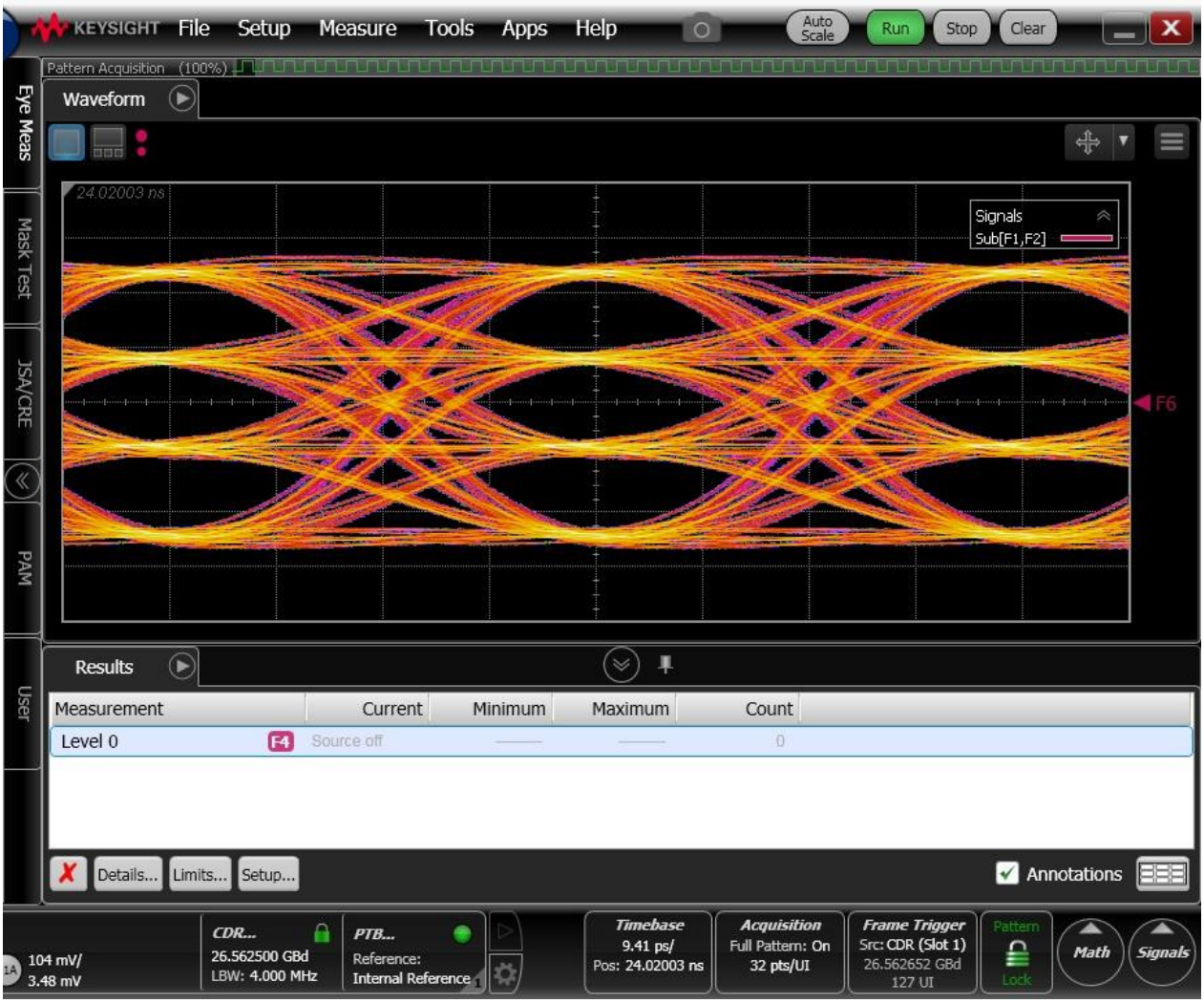


Figure 6: PAM4 DSP TX lane eye with a quartz clock generator driving each of the two reference clock inputs independently.

The jitter performance parameters for the PAM4 DSP TX lane are shown in Figure 7.

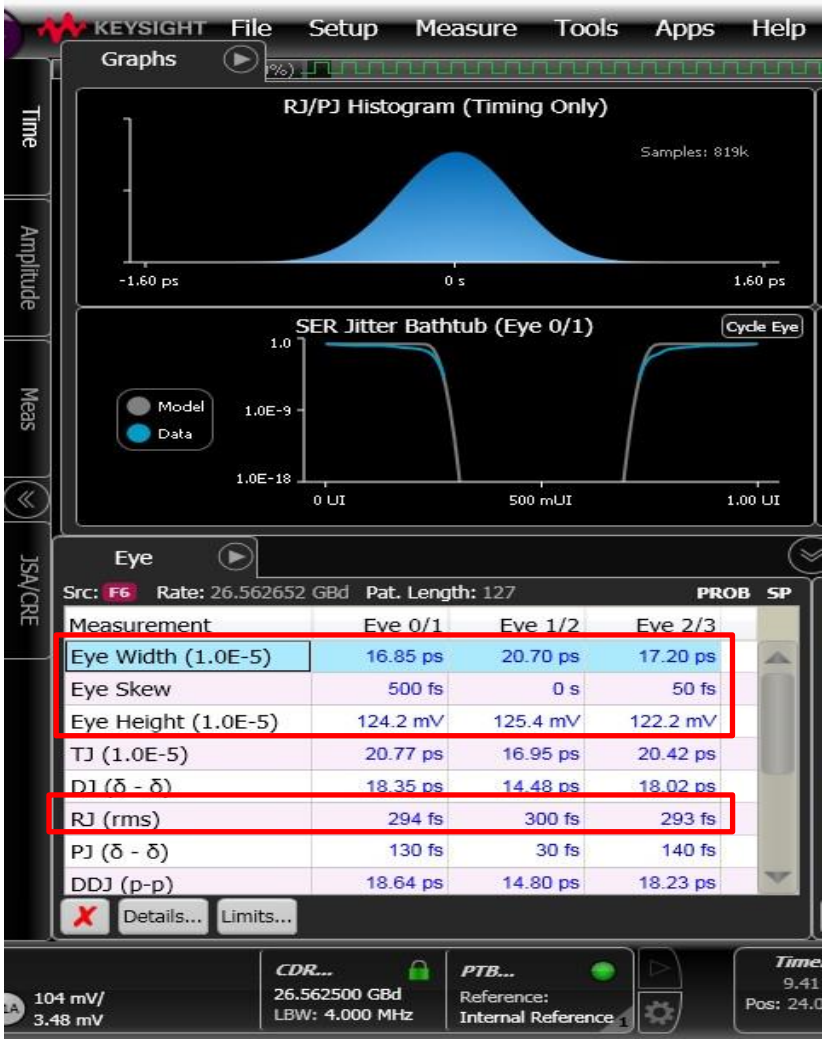


Figure 7: PAM4 DSP TX-1 data lane jitter performance parameters with a quartz clock generator driving each of the two reference-clock inputs.

Note that the reference clock contribution to the PHY TX lane eye is indicated by the following measured parameters:

1. Eye width
2. Eye skew
3. Eye height
4. SER jitter bathtub
5. RJ

5 Conclusion

The measurement data show that the SiTime SiT9365 MEMS LVPECL oscillator can drive two reference clock inputs of the Inphi 400G PAM4 DSP with no degradation in eye opening or jitter/noise performance.

Table-3: Eye/Jitter performance of a CD12 TX lane

Performance Parameters	One MEMS SiT9365 Oscillator Eye 0/1	Two Quartz Clock Sources Eye 0/1
Eye width (ps)	17.4	16.85
Eye skew (fs)	300	500
Eye height (mV)	131.8	124.2
RJ, rms (fs)	266	294
Clock IDD (mA) without termination load	85	130*

**In a real application, if a clock generator or a single SiT9365 was not used, the alternative would have been two separate differential oscillators each consuming a minimum of 65 mA for a total of 130 mA.*

The RJ (rms) component of the total jitter measurement is a key indicator of the reference clock contribution. In this test scenario, the MEMS SiT9365 oscillator outperforms the quartz clock generator used on the EVB as shown in Table 3.

In an SFP module, it is more common to use two oscillators instead of one clock generator for power, space and cost reasons. However, using one SiTime SiT9365-156.25 MHz oscillator, which can effectively drive two differential loads, versus two separate differential oscillators saves additional board space and BOM cost. In addition, the sub-system power dissipation and EMI/RFI is reduced because there is only one oscillator in the design and one differential pair of clock traces on the board.

6 References:

[1] Inphi PAM4 DSP datasheet: IN015050-CD02; https://www.inphi.com/.

[2] SiTime SiT9365 datasheet; https://www.sitime.com/products/lvpecl-lvds-hcsl-oscillators/sit9365.

Table 4: Revision History

Version	Release Date	Change Summary
1.0	08/29/2018	Original doc

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