SiT9514x Dynamic Control of Outputs

1 Introduction

This application note details the dynamic output enable and disable configuration for all the outputs.

2 Procedure for Pseudo Code

- Fast Variable: enable (0 – OFF ; 1 – ON)
- For normal I2C writes
    - i2c.i2cw(slave address, register address, data)
- For writing a data to a particular bit (or no of bits) in a register
    - i2c.i2crmw(slave address, register address, start_bit, no_of_bits, data)
- For example, i2c.i2crmw (0x69, 0xF3, 2, 3, 0).
    - Slave address : 0x69
    - Register address : 0xF3
    - Start bit [MSB]
    - No. of bits that need to be changed from start bit (In this example its 3 bits that need to be changed [2:0])
    - Register data (That will change only for the selected no of bits).

3 SiT95141/43/45/48 Output Enable and Disable Configuration

3.1 For differential outputs

Table 1: Psuedo Code for Differential Outputs

Output	Pseudo Code
OUT0BP & OUT0BN	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF4,2,1,1) i2c.i2crmw(0x69,0xF5,2,1,enable)
OUT0TP & OUT0TN	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF4,0,1,1) i2c.i2crmw(0x69,0xF5,0,1,enable)
OUT7P & OUT7N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,7,1,1) i2c.i2crmw(0x69,0xF3,7,1,enable)
OUT6P & OUT6N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,6,1,1) i2c.i2crmw(0x69,0xF3,6,1,enable)
OUT5P & OUT5N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,5,1,1) i2c.i2crmw(0x69,0xF3,5,1,enable)
OUT4P & OUT4N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,4,1,1) i2c.i2crmw(0x69,0xF3,4,1,enable)
OUT3P & OUT3N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,3,1,1) i2c.i2crmw(0x69,0xF3,3,1,enable)
OUT2P & OUT2N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,2,1,1) i2c.i2crmw(0x69,0xF3,2,1,enable)
OUT1P & OUT1N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,1,1,1) i2c.i2crmw(0x69,0xF3,1,1,enable)
OUT0P & OUT0N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,0,1,1) i2c.i2crmw(0x69,0xF3,0,1,enable)

3.2 For SE – P side

Table 2: Psuedo Code for SE – P side

Output	Pseudo Code
OUT0BP	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xFA,2,1,1) i2c.i2crmw(0x69,0xFB,2,1,enable)
OUT0TP	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xFA,0,1,1) i2c.i2crmw(0x69,0xFB,0,1,enable)
OUT7P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,7,1,1) i2c.i2crmw(0x69,0xF9,7,1,enable)
OUT6P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,6,1,1) i2c.i2crmw(0x69,0xF9,6,1,enable)
OUT5P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,5,1,1) i2c.i2crmw(0x69,0xF9,5,1,enable)
OUT4P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,4,1,1) i2c.i2crmw(0x69,0xF9,4,1,enable)
OUT3P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,3,1,1) i2c.i2crmw(0x69,0xF9,3,1,enable)
OUT2P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,2,1,1) i2c.i2crmw(0x69,0xF9,2,1,enable)
OUT1P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,1,1,1) i2c.i2crmw(0x69,0xF9,1,1,enable)
OUT0P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,0,1,1) i2c.i2crmw(0x69,0xF9,0,1,enable)

3.3 For SE – N side

Table 3 Psuedo Code for SE- N Side

Output	Pseudo Code
OUT0BN	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF4,6,1,1) i2c.i2crmw(0x69,0xF5,6,1,enable)
OUT0TN	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF4,4,1,1) i2c.i2crmw(0x69,0xF5,4,1,enable)
OUT7N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,7,1,1) i2c.i2crmw(0x69,0xF7,7,1,enable)
OUT6N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,6,1,1) i2c.i2crmw(0x69,0xF7,6,1,enable)
OUT5N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,5,1,1) i2c.i2crmw(0x69,0xF7,5,1,enable)
OUT4N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,4,1,1) i2c.i2crmw(0x69,0xF7,4,1,enable)
OUT3N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,3,1,1) i2c.i2crmw(0x69,0xF7,3,1,enable)
OUT2N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,2,1,1) i2c.i2crmw(0x69,0xF7,2,1,enable)
OUT1N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,1,1,1) i2c.i2crmw(0x69,0xF7,1,1,enable)
OUT0N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,0,1,1) i2c.i2crmw(0x69,0xF7,0,1,enable)

4 SiT95147 Output Enable and Disable Configuration

4.1 For differential outputs

Table 4 Pseudo Code for Differential Outputs

Output	Pseudo Code
OUT0BP & OUT0BN	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF4,2,1,1) i2c.i2crmw(0x69,0xF5,2,1,enable)
OUT0TP & OUT0TN	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF4,0,1,1) i2c.i2crmw(0x69,0xF5,0,1,enable)
OUT7P & OUT7N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,7,1,1) i2c.i2crmw(0x69,0xF3,7,1,enable)
OUT6P & OUT6N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,6,1,1) i2c.i2crmw(0x69,0xF3,6,1,enable)
OUT5P & OUT5N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,5,1,1) i2c.i2crmw(0x69,0xF3,5,1,enable)
OUT3P & OUT3N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,3,1,1) i2c.i2crmw(0x69,0xF3,3,1,enable)
OUT2P & OUT2N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,2,1,1) i2c.i2crmw(0x69,0xF3,2,1,enable)
OUT1P & OUT1N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF2,1,1,1) i2c.i2crmw(0x69,0xF3,1,1,enable)

4.2 For SE mode - P side

Table 5 Psuedo Code for SE - P side

Output	Pseudo Code
OUT0BP	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xFA,2,1,1) i2c.i2crmw(0x69,0xFB,2,1,enable)
OUT0TP	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xFA,0,1,1) i2c.i2crmw(0x69,0xFB,0,1,enable)
OUT7P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,7,1,1) i2c.i2crmw(0x69,0xF9,7,1,enable)
OUT6P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,6,1,1) i2c.i2crmw(0x69,0xF9,6,1,enable)
OUT5P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,5,1,1) i2c.i2crmw(0x69,0xF9,5,1,enable)
OUT3P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,3,1,1) i2c.i2crmw(0x69,0xF9,3,1,enable)
OUT2P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,2,1,1) i2c.i2crmw(0x69,0xF9,2,1,enable)
OUT1P	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF8,1,1,1) i2c.i2crmw(0x69,0xF9,1,1,enable)

4.3 For SE mode - N side

Table 6 Psuedo Code for SE - N side

Output	Pseudo Code
OUT0BN	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF4,6,1,1) i2c.i2crmw(0x69,0xF5,6,1,enable)
OUT0TN	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF4,4,1,1) i2c.i2crmw(0x69,0xF5,4,1,enable)
OUT7N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,7,1,1) i2c.i2crmw(0x69,0xF7,7,1,enable)
OUT6N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,6,1,1) i2c.i2crmw(0x69,0xF7,6,1,enable)
OUT5N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,5,1,1) i2c.i2crmw(0x69,0xF7,5,1,enable)
OUT3N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,3,1,1) i2c.i2crmw(0x69,0xF7,3,1,enable)
OUT2N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,2,1,1) i2c.i2crmw(0x69,0xF7,2,1,enable)
OUT1N	i2c.i2cw(0x69,0xff,0x03) i2c.i2crmw(0x69,0xF6,1,1,1) i2c.i2crmw(0x69,0xF7,1,1,enable)

Table 2: Revision History

Version	Release Date	Change Summary
1.0	01/19/2020	Original doc

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