	<b>Title:</b>	Performance report for SiT9366, 53.125 MHz, HCSL		
	<b>Type:</b>	Performance report	<b>Rev:</b>	1.0
	<b>Orig:</b>		<b>Date:</b>	April 16, 2018

## Performance report for SiT9366 - 53.125 MHz, HCSL

### Conditions:


- Frequency 53.125 MHz
- VDD: 2.5 V, 3.3 V
- Room temperature
- Termination:
  - o 30  $\Omega$  series and 50  $\Omega$  to GND.

### Equipment:

Model	Measurement / Purpose
Keysight DSA90604A (6 GHz, 20 Gbps)	Period jitter, differential voltage swing, rise/fall time, duty cycle
Keysight 5052B Signal Source Analyzer	Phase noise, integrated phase jitter
Keysight 34980A	Power supply current
Keysight E3631A	Power supply
Keysight 53230A	Frequency

### Test setup:

For waveform parameters measurement (rise/fall time, differential swing, duty cycle), both DUT outputs are terminated with 30  $\Omega$  series and 50  $\Omega$  to GND. Output signals are measured using Keysight 1134B active probe with Keysight N5425B probe head. All measurements are applied to the differential waveform. Figure 1 shows test setup diagram for waveform parameters measurement.

	<b>Title:</b>	Performance report for SiT9366, 53.125 MHz, HCSL		
	<b>Type:</b>	Performance report	<b>Rev:</b>	1.0
	<b>Orig:</b>		<b>Date:</b>	April 16, 2018

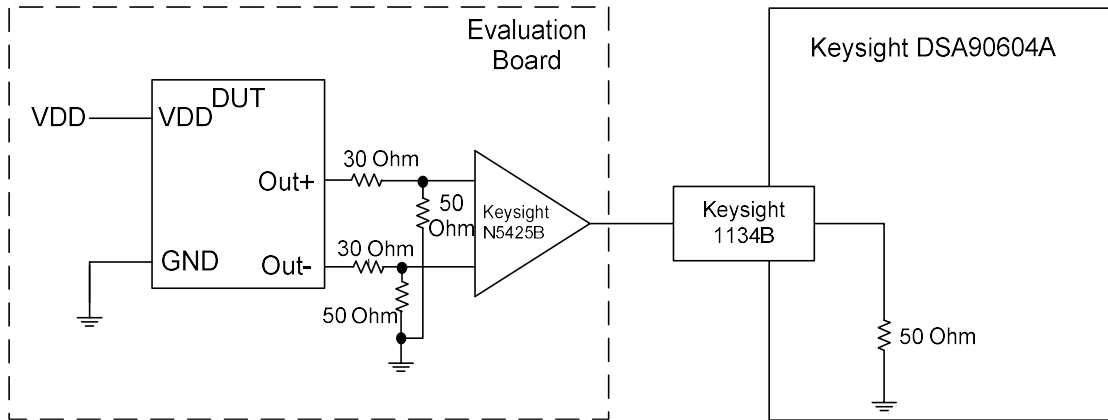


Figure 1: Test setup for measuring waveform parameters (rise/fall time, differential swing, duty cycle)

For period jitter measurement output is terminated with 30  $\Omega$  series and 50  $\Omega$  to GND at the input of hi-speed comparator (ADCMP581). AC coupled comparator's output is connected to oscilloscope channel. Figure 2 shows test setup diagram for period jitter measurement.



Figure 2: Test setup for measuring period jitter

For phase noise measurements, differential signal is converted to single-ended using impedance matching transformer. Transformer's output is connected to measurement instrument. Output is also terminated with 30  $\Omega$  series at the source side. Figure 3 shows test setup diagram for phase noise measurement.

<b>SiTime</b>	<b>Title:</b>	<b>Performance report for SiT9366, 53.125 MHz, HCSL</b>		
	<b>Type:</b>	<b>Performance report</b>	<b>Rev:</b>	<b>1.0</b>
	<b>Orig:</b>		<b>Date:</b>	<b>April 16, 2018</b>



Figure 3: Test setup for measuring phase noise.

For IDD measurement device output is floating. For frequency measurement differential-to-single-ended converter is used.

**Data:**

- Phase noise
- Integrated phase jitter
- RMS period jitter
- Peak-to-peak period jitter
- Rise/fall time
- Duty cycle
- Differential output swing
- IDD
- Frequency stability over temperature

Table 1: Summary performance data

Parameter	Units	Voltage	
		2.5 V	3.3 V
Integrated Phase jitter (1.875 MHz - 20 MHz)	fs, rms	136	134
Integrated Phase jitter (12 kHz - 20 MHz)	fs, rms	231	230
Period jitter	ps, rms	1.04	1.01
Period jitter (10,000 cycles)	ps, pk-pk	8.02	7.90
Duty cycle	%	50.0	50.0
Rise time (20% - 80%)	ps	366	363
Fall time (80% - 20%)	ps	372	368
Differential voltage swing	V	1.33	1.40
Current consumption (no load, output enabled)	mA	74.9	75.5
Current consumption (no load, output disabled)	mA	51.2	51.6

The information contained in this document is confidential and proprietary to SiTime Corporation. Unauthorized reproduction or distribution is prohibited.

<b>SiTime</b>	<b>Title:</b>	Performance report for SiT9366, 53.125 MHz, HCSL		
	<b>Type:</b>	Performance report	<b>Rev:</b>	1.0
	<b>Orig:</b>		<b>Date:</b>	April 16, 2018

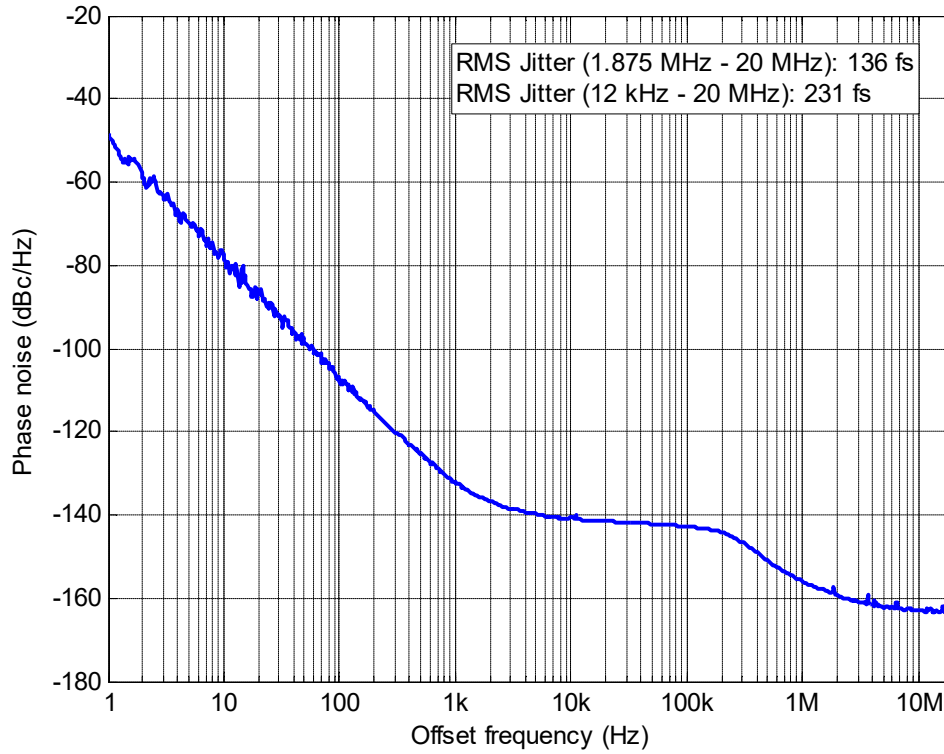


Figure 4: Phase noise, 2.5 V

The information contained in this document is confidential and proprietary to SiTime Corporation. Unauthorized reproduction or distribution is prohibited.

<b>SiTime</b>	<b>Title:</b>	Performance report for SiT9366, 53.125 MHz, HCSL		
	<b>Type:</b>	Performance report	<b>Rev:</b>	1.0
	<b>Orig:</b>		<b>Date:</b>	April 16, 2018

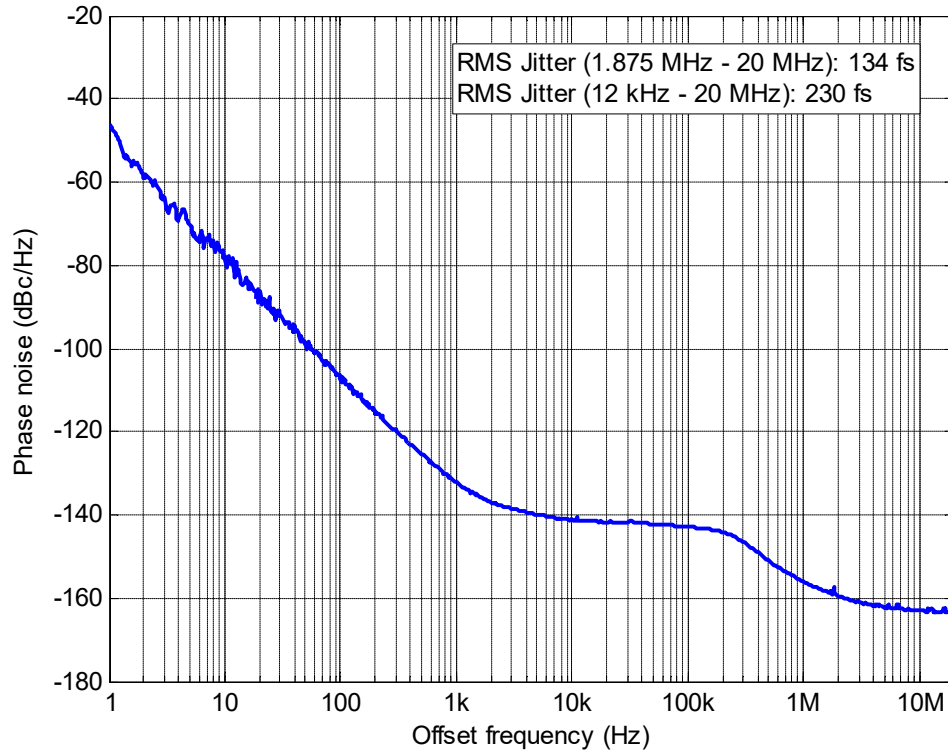


Figure 5: Phase noise, 3.3 V

The information contained in this document is confidential and proprietary to SiTime Corporation. Unauthorized reproduction or distribution is prohibited.

<b>SiTime</b>	<b>Title:</b>	Performance report for SiT9366, 53.125 MHz, HCSL		
	<b>Type:</b>	Performance report	<b>Rev:</b>	1.0
	<b>Orig:</b>		<b>Date:</b>	April 16, 2018



Figure 6: Output waveform, 2.5 V


	<b>Title:</b>	Performance report for SiT9366, 53.125 MHz, HCSL		
	<b>Type:</b>	Performance report	<b>Rev:</b>	1.0
	<b>Orig:</b>		<b>Date:</b>	April 16, 2018



Figure 7: Output waveform, 3.3 V

The information contained in this document is confidential and proprietary to SiTime Corporation. Unauthorized reproduction or distribution is prohibited.

<b>SiTime</b>	<b>Title:</b>	Performance report for SiT9366, 53.125 MHz, HCSL		
	<b>Type:</b>	Performance report	<b>Rev:</b>	1.0
	<b>Orig:</b>		<b>Date:</b>	April 16, 2018

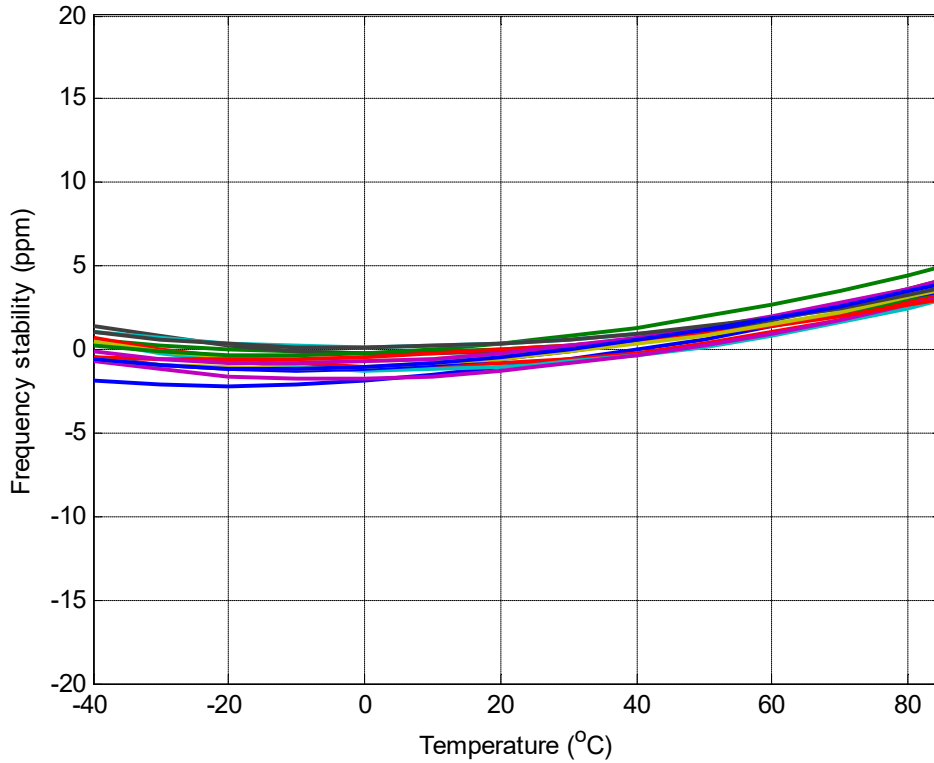


Figure 8: Frequency stability\* over temperature, 2.5 V

\*SiT9366 frequency stability is independent of output frequency.

**The information contained in this document is confidential and proprietary to SiTime Corporation. Unauthorized reproduction or distribution is prohibited.**



<b>SiTime</b>	<b>Title:</b>	Performance report for SiT9366, 53.125 MHz, HCSL		
	<b>Type:</b>	Performance report	<b>Rev:</b>	1.0
	<b>Orig:</b>		<b>Date:</b>	April 16, 2018

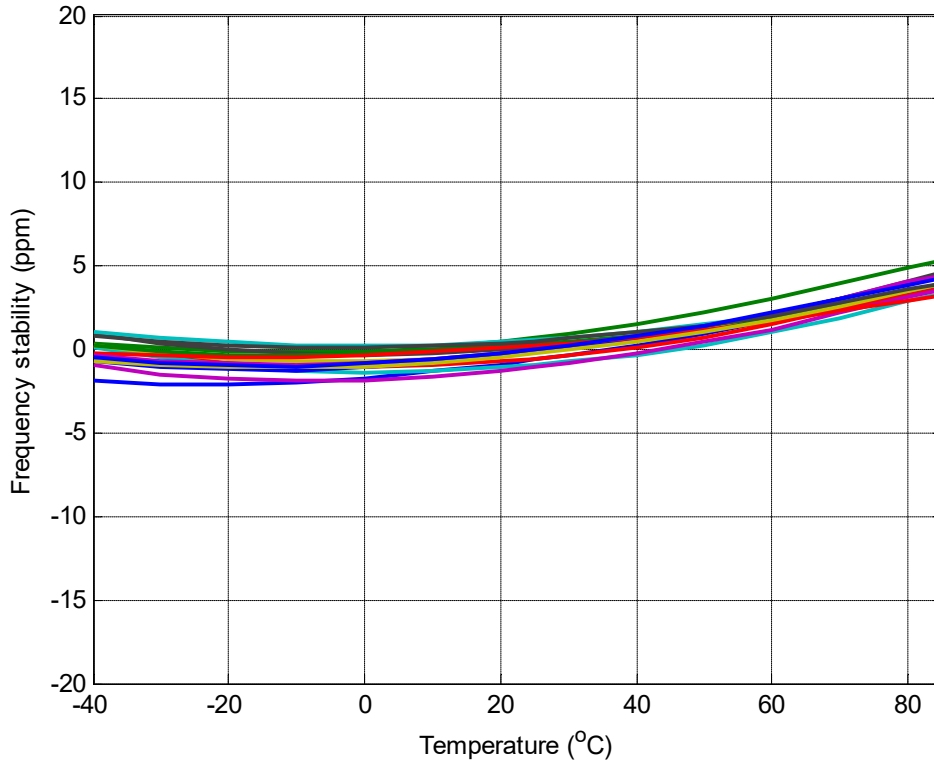


Figure 9: Frequency stability over temperature, 3.3 V

**The information contained in this document is confidential and proprietary to SiTime Corporation. Unauthorized reproduction or distribution is prohibited.**