	<b>Title:</b>	Performance report for SiT9366, 106.25 MHz, LVPECL		
	<b>Type:</b>	Performance report	<b>Rev:</b>	1.0
	<b>Orig:</b>		<b>Date:</b>	April 16, 2018

## Performance report for SiT9366 - 106.25 MHz, LVPECL

### Conditions:


- Frequency 106.25 MHz
- VDD: 2.5 V, 3.3 V
- Room temperature
- Termination:
  - o 50  $\Omega$  to VDD – 2 V.

### Equipment:

Model	Measurement / Purpose
Keysight DSA90604A (6 GHz, 20 Gbps)	Period jitter, differential voltage swing, rise/fall time, duty cycle
Keysight 5052B Signal Source Analyzer	Phase noise, integrated phase jitter
Keysight 34980A	Power supply current
Keysight E3631A	Power supply
Keysight 53230A	Frequency

### Test setup:

For waveform parameters measurement (rise/fall time, differential swing, duty cycle), both DUT outputs are terminated with 50  $\Omega$  to VDD - 2 V. Output signals are measured using Keysight 1134B active probe with Keysight N5425B probe head. All measurements are applied to the differential waveform. Figure 1 shows test setup diagram for waveform parameters measurement.

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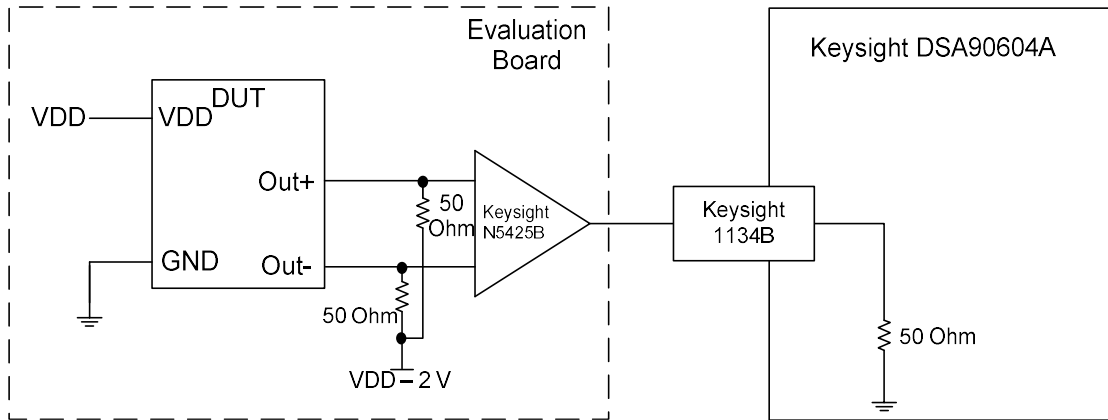


Figure 1: Test setup for measuring waveform parameters (rise/fall time, differential swing, duty cycle)

For period jitter measurement output is terminated with  $50 \Omega$  to  $VDD - 2 V$  at the input of hi-speed comparator (ADCMP581). AC coupled comparator's output is connected to oscilloscope channel. Figure 2 shows test setup diagram for period jitter measurement.



Figure 2: Test setup for measuring period jitter

For phase noise measurements, differential signal is converted to single-ended using impedance matching transformer. Transformer's output is connected to measurement instrument. Output is also terminated with  $30 \Omega$  series at the source side. Figure 3 shows test setup diagram for phase noise measurement.

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Figure 3: Test setup for measuring phase noise.

For IDD measurement device output is floating. For frequency measurement differential-to-single-ended converter is used.

**Data:**

- Phase noise
- Integrated phase jitter
- RMS period jitter
- Peak-to-peak period jitter
- Rise/fall time
- Duty cycle
- Differential output swing
- IDD
- Frequency stability over temperature

Table 1: Summary performance data

Parameter	Units	Voltage	
		2.5 V	3.3 V
Integrated Phase jitter (1.875 MHz - 20 MHz)	fs, rms	130	131
Integrated Phase jitter (12 kHz - 20 MHz)	fs, rms	229	235
Period jitter	ps, rms	1.07	1.06
Period jitter (10,000 cycles)	ps, pk-pk	8.46	8.41
Duty cycle	%	50.1	50.1
Rise time (20% - 80%)	ps	253	244
Fall time (80% - 20%)	ps	252	241
Differential voltage swing	V	1.61	1.59
Current consumption (no load, output enabled)	mA	75.2	75.5
Current consumption (no load, output disabled)	mA	49.5	49.6

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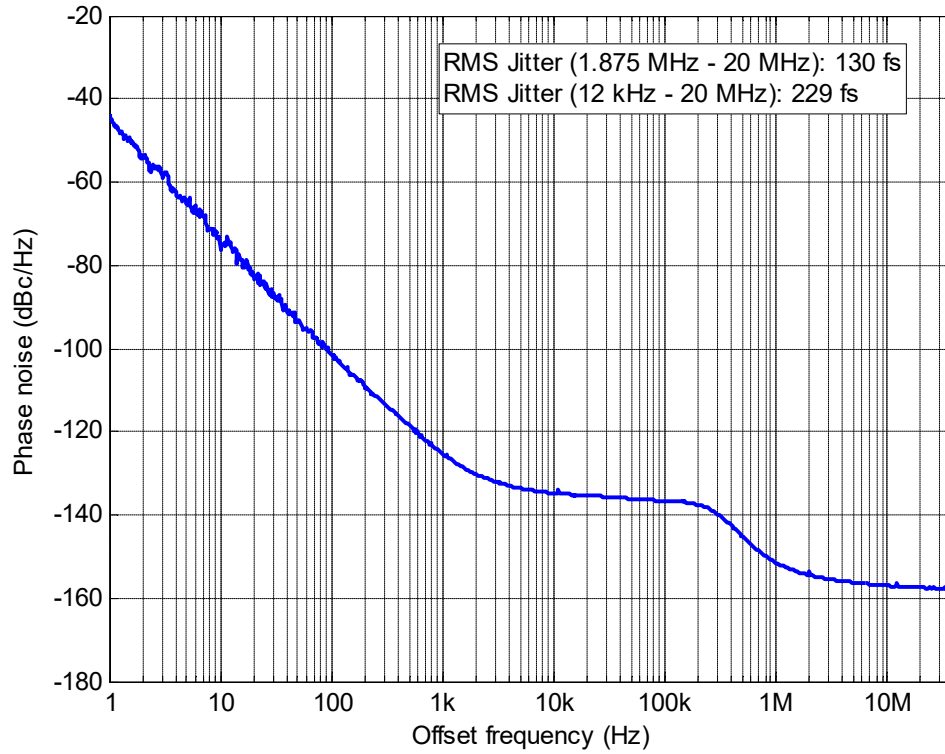


Figure 4: Phase noise, 2.5 V

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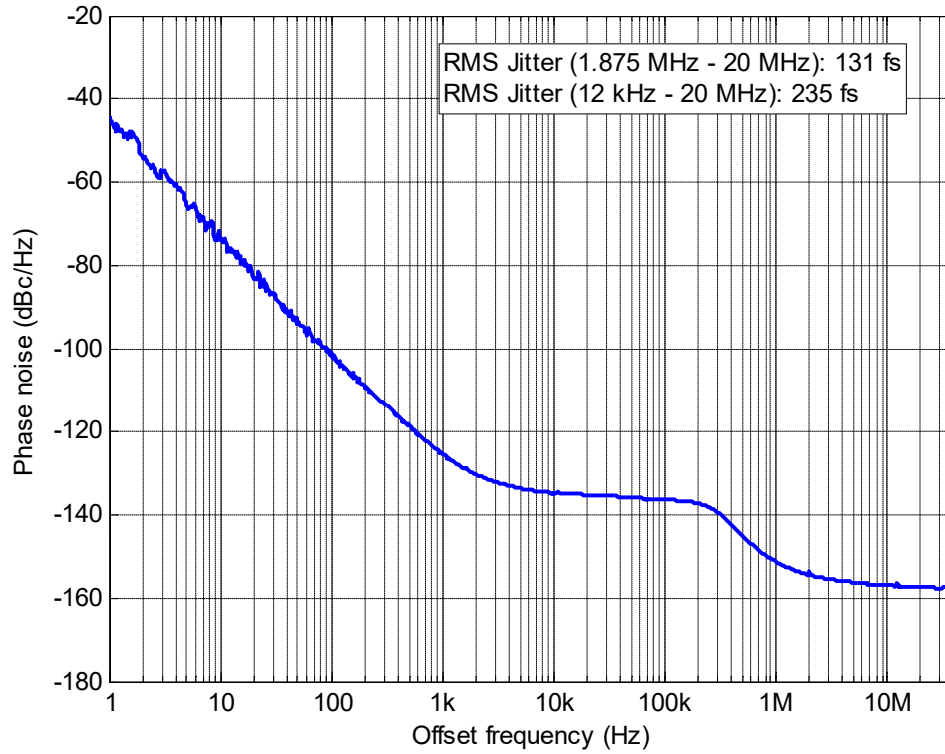


Figure 5: Phase noise, 3.3 V

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Figure 6: Output waveform, 2.5 V

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Figure 7: Output waveform, 3.3 V

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Figure 8: Frequency stability\* over temperature, 2.5 V

\*SiT9366 frequency stability is independent of output frequency.

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Figure 9: Frequency stability over temperature, 3.3 V

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