Time Error Simulation – Software and Models

A vital role in time synchronization and 5G/comms applications

Since the advent of the telecom industry, network synchronization has been an important factor for voice communications. Early on, frequency synchronization was adopted to ensure high quality and highly reliable telephone calls. In today's networks, data traffic consumes the bulk of the network bandwidth. Although voice communications now comprise a small fraction of network bandwidth, frequency and time/phase synchronization are still required to ensure network operation and reliability.

Time synchronization became important when networks started using time division duplexing (TDD). With the forthcoming rollout of 5G, very tight time/phase synchronization, along with frequency synchronization, will be essential for these networks to improve data throughput to support the demands of emerging applications such as autonomous driving, remote surgery, and more precise geolocation.

The local oscillator that is located in a network node plays an essential role in the overall synchronization performance of the system. This holds true for frequency synchronized systems using Synchronous Ethernet, a time/phase/frequency synchronized system using precision time protocol (PTP) described in IEEE 1588, or a combination of both. In 5G networks, stringent time alignment requirements are of utmost importance across the entire system. The alignment requirement at the base station antenna can be very tight, as low as 65 nanoseconds (ns) depending on MIMO, carrier aggregation, and transmitter diversity. Additionally, the amount of added timing error allowed by each network node in the backhaul network (network switch, router) can be as low as 5 ns per node.

In such synchronization systems there is a local oscillator at each network node which provides a clock-to-synchronization phase locked loop (PLL). The PLL loop bandwidth is typically set in the range from 1 mHz to 0.1 Hz depending on the implementation. A number of factors impact time error performance. The stability of the local oscillator is the main contributor to the time error generated in the node. PLL filtering capabilities (PLL loop order, PLL loop bandwidth) and the amount of wander in the input signals are also contributing factors.

Actual time error analysis using real-time data is a complex and lengthy process to perform ranging from weeks to months. To help alleviate these issues, SiTime has developed Time Error Simulator software that simulates how much wander is generated by the instabilities of the local oscillator, provided that reference inputs are ideal and wander free. This tool enables quick simulation of time error under a variety of different system parameters and temperature profiles.

SiTime Time Error Simulator software requires the following three areas of basic performance data for the oscillator (measured on the component level):

1. Frequency over temperature behavior of the oscillator – to simulate the temperature change contribution.
2. Frequency over time behavior of the oscillator (at least 1 hour of frequency trend) – to simulate the wander contribution of the oscillator.
3. One-day frequency aging – to simulate the aging contribution of the oscillator.

This data can be obtained in the lab with no more than one day of data capture. Or, it can be provided by the oscillator vendor. Depending on the performance of the user's PC, the 24-hour frequency aging can take as little as a half an hour of simulation time, which is significantly faster than taking real-time measurements.

This paper discusses a variety of models used for time error simulation for PTP and PTP + SyncE applications using Time Error Simulator software.

1. PTP-only Simulation Model

PTP-only simulation mode simulates the impact of local oscillator frequency variation on the performance of a single telecom clock (like a T-BC) that does not have physical layer frequency support. The model in this case is a single PLL model.

Time Error Simulator software supports simulation of system locked state. Figure 1 illustrates the simulation model diagram.

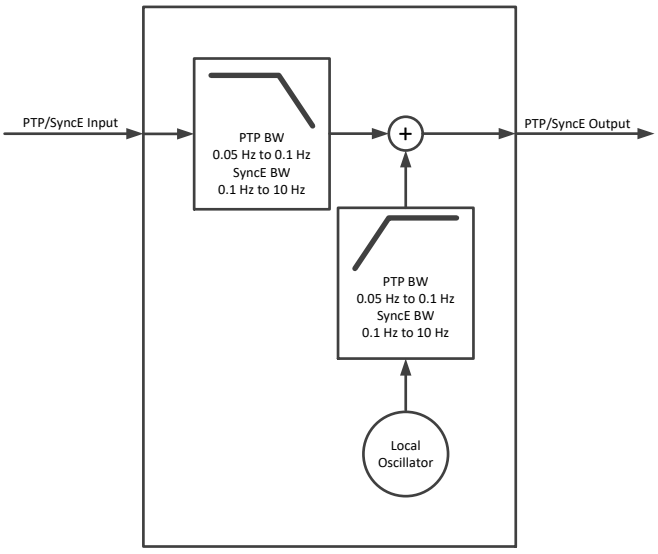

Figure 1: PTP system node simulation model

Input to the PLL model is the frequency behavior over time of the local oscillator. A number of

contributors to the frequency variation of the local oscillator can be selected: variable temperature effect, oscillator wander effect, and daily aging effect. Details of the simulation of oscillator behavior are discussed in Section 3.

For locked state simulation, PTP input is assumed to be ideal and therefore time error is 0. This approach is used to simulate the contribution of local oscillator instability. The frequency over time trend of the local oscillator is used to calculate a frequency error from the ideal clock. This frequency error is integrated to calculate the time error. Then, the model of a local oscillator contribution to a PLL output is applied to time error to simulate the resulting time error of the PLL output. A simplified model of a local oscillator impact on a PLL output is a high pass filter with cutoff frequency which is the same as a loop filter bandwidth. Filter bandwidth and order parameters are defined by the user.

PTP-only simulation mode can also be used to estimate SyncE eEEC performance, since the software generates generic PLL simulation. However, the clock bandwidth will be different. In telecommunication applications, PTP bandwidth usually ranges from a few mHz to 20 mHz, and SyncE bandwidth is within 0.1 Hz to 10 Hz.

2. Hybrid (PTP + SyncE) Simulation Model

Hybrid (PTP + SyncE) simulation mode simulates the impact of a local oscillator on the performance of either a single T-BC or a chain of T-BCs. This model assumes hybrid T-BC where physical layer frequency support is provided over SyncE. The software implements locked state simulation.

Figure 2 shows a model of T-BC defined in G.8273.2. Figure 3 shows a simulation model of T-BC implemented in the software.

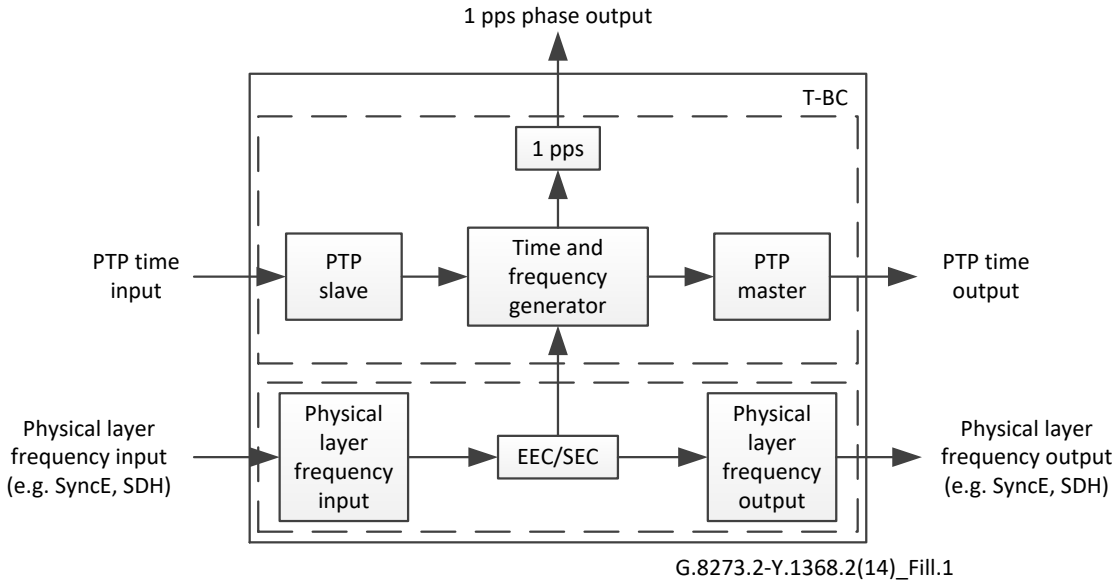

Figure 2: Model of the T-BC defined in G.8273.2

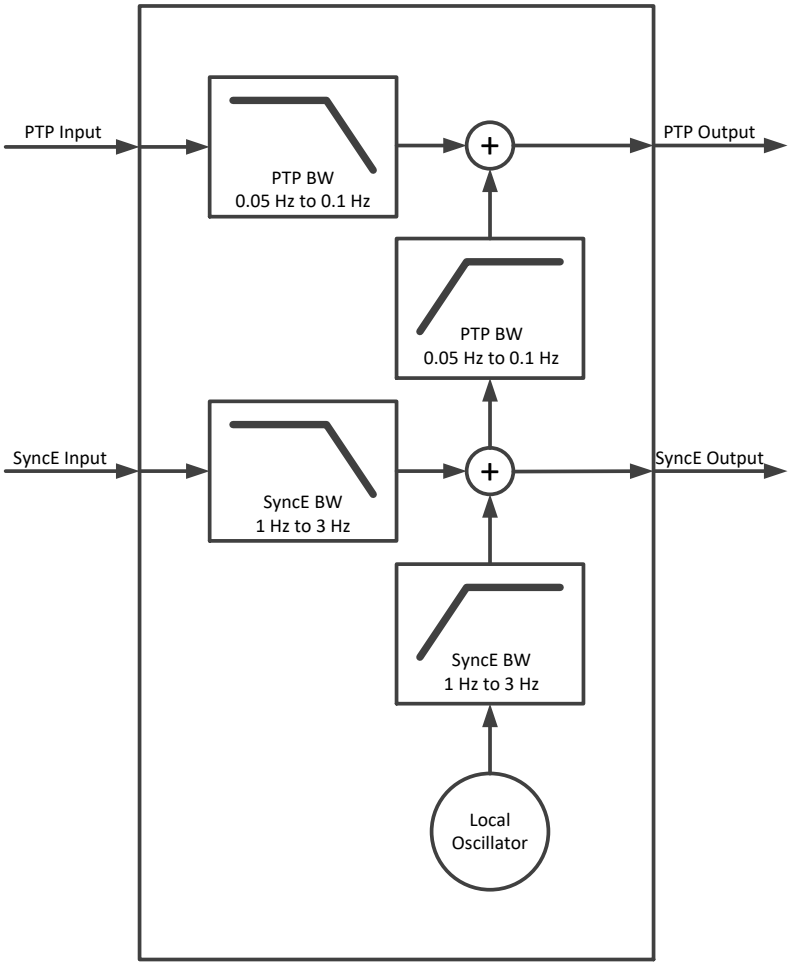

Figure 3: Simulation Model of the T-BC implemented in the software

The frequency behavior over time of the local oscillator is the same as in the PTP-only simulation input to the T-BC model. Both PTP grandmaster and SyncE primary reference clock are assumed to be ideal. In chain simulation, PTP and SyncE inputs to the node are corresponding outputs from the previous node. Local oscillator behavior is assumed to be the same for all T-BCs in the chain.

The frequency over time trend measurement of the local oscillator is used to calculate a frequency error from the ideal clock. This frequency error is integrated to calculate the time error. Then, the model of a local oscillator contribution to a T-BC output is applied to time error to simulate the resulting time error of the T-BC output. T-BC is simulated as two cascaded PLLs – SyncE PLL and PTP PLL (see Figure 4). Output of the SyncE PLL is a reference to a PTP PLL.

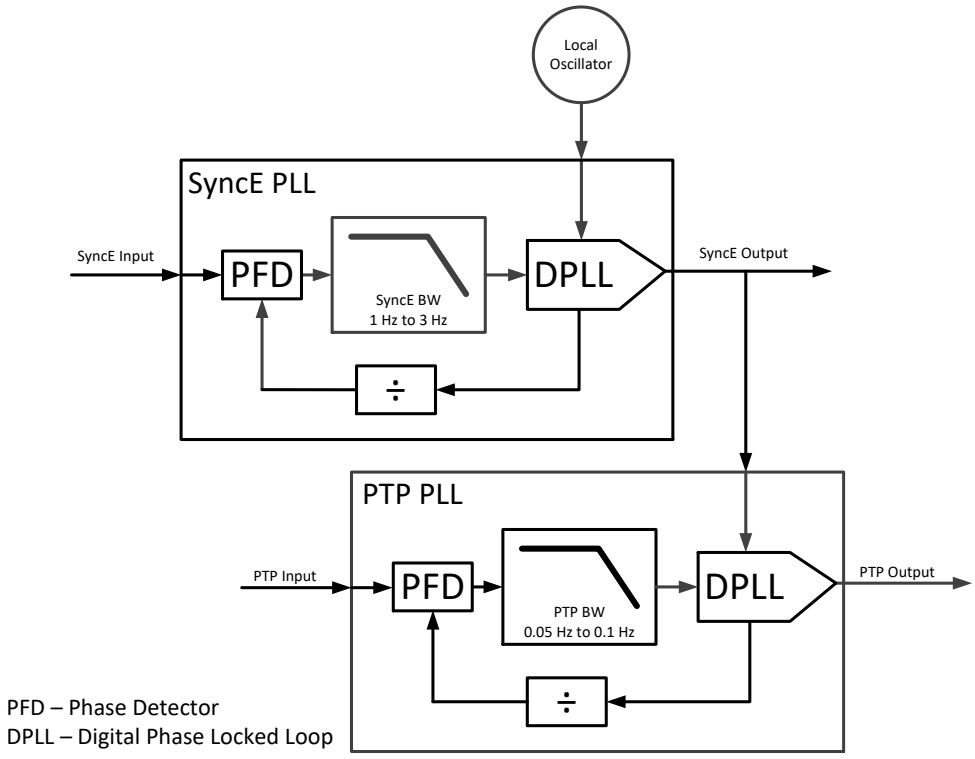

Figure 4: SyncE-PTP PLL cascade

As illustrated in Figure 3, the transfer function of oscillator time error to SyncE output is approximated by a high-pass filter with a bandwidth equal to SyncE bandwidth. The transfer function of SyncE input time error to SyncE output time error is approximated by a low-pass filter with the same bandwidth.

SyncE can be viewed as a local oscillator for a PTP block of T-BC. To model the PTP PLL, the same concept in the case of SyncE PLL is used: a high pass transfer function with respect to local oscillator contribution (SyncE output) and a low-pass transfer function with respect to PTP input contribution.

3. Simulation of Local Oscillator Frequency Variation

The contribution of various factors to the time error of the local oscillator can be simulated with Time Error Simulator software. These factors are:

1. Variable temperature
2. Wander of an oscillator
3. Daily aging

In a typical case, the resulting contribution of all these factors is simulated to address the real-life scenario. But the contribution of each factor separately can be simulated as well. Figure 5 shows simulation model for each of the different factors mentioned above.

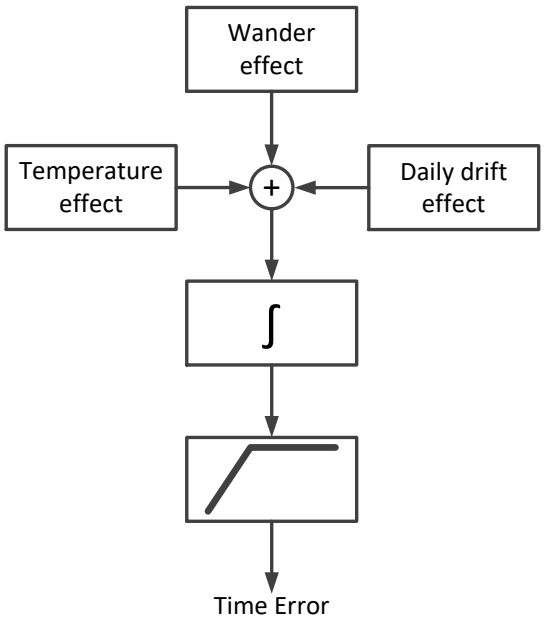

Figure 5: Simulation models of oscillator's time error contributing factors

Frequency over time trends representing each of the contributing factors are added together to calculate the overall frequency variation. Then, it is integrated to calculate time error. Time error gets filtered with hi-pass filter representing the system response to local oscillator instability.

Input data models for each factor are discussed in more detail in the following sections.

3.1. Variable Temperature

Simulation of variable temperature contribution requires two inputs:

1. Frequency over temperature characteristic of the oscillator of interest
2. Temperature profile in time representing temperature change during simulation period

Figure 6 shows a block diagram of the variable temperature simulation model.

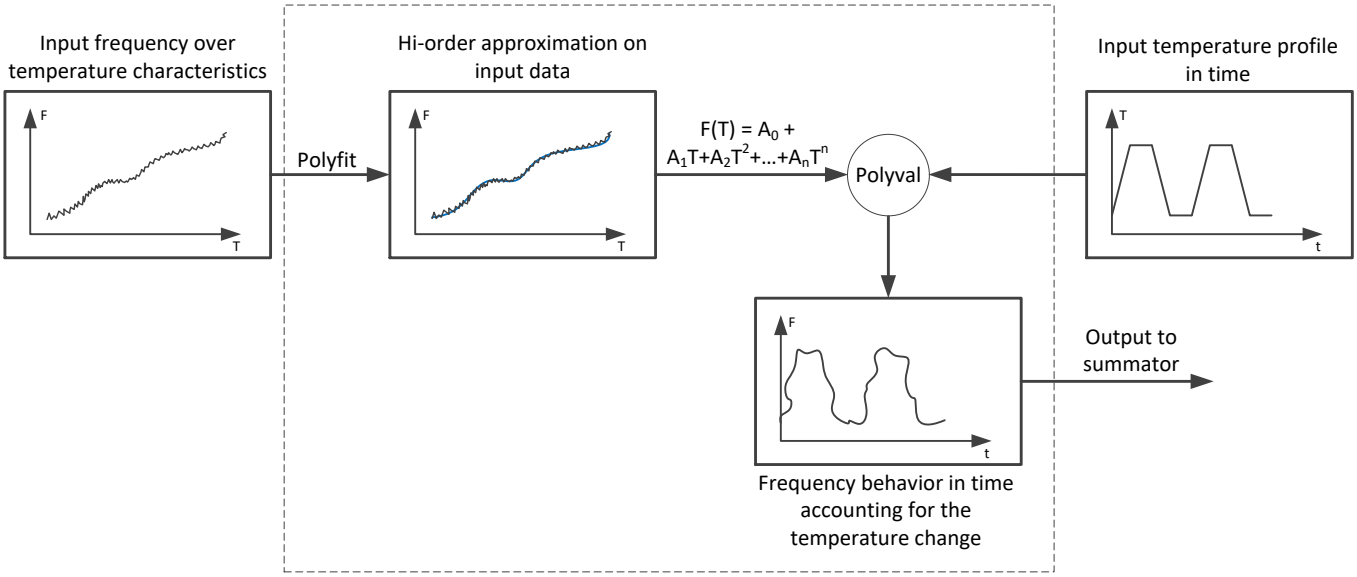

Figure 6: Variable temperature effect simulation model

Frequency over temperature data of the oscillator is modeled with a high order polynomial. This polynomial is used to calculate frequency in time behavior from the temperature profile data. The resulting frequency over time characteristics is an environment temperature contribution that must be included with the other factors (Figure 5).

3.2. Clock Wander

Simulation of clock wander contribution requires frequency behavior in time of the oscillator of interest (frequency trend) as an input. Figure 7 shows a block diagram of the clock wander simulation model.

The input frequency trend is fitted with a straight line which represents daily aging of the oscillator. It is further subtracted from the input data because daily drift is calculated separately. Output of the model is added with the other factors.

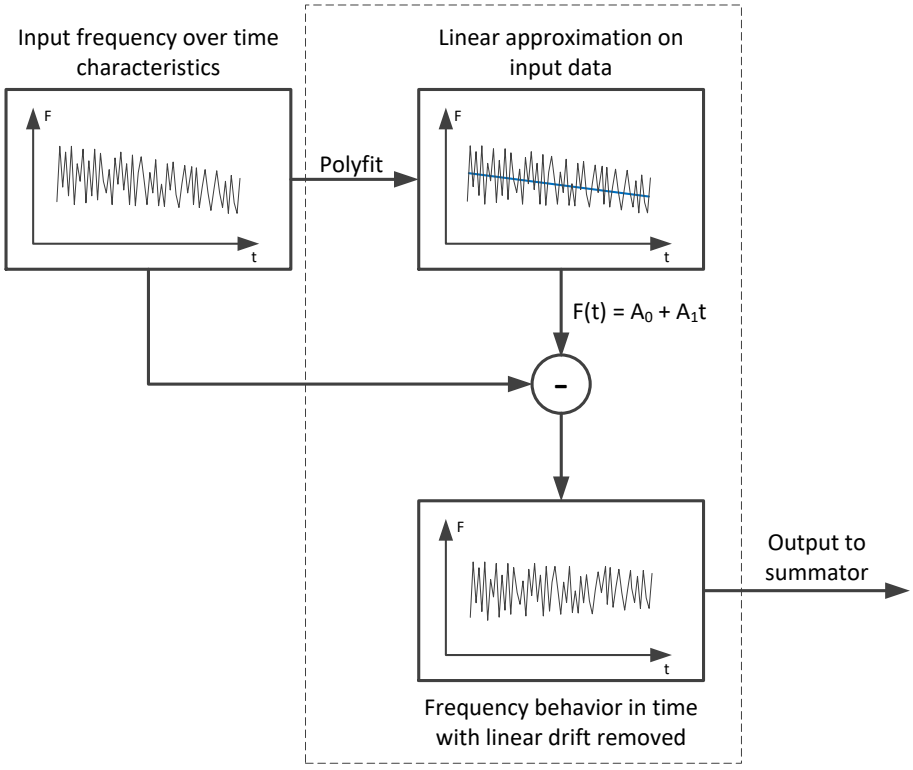

Figure 7: Clock wander simulation model

3.3. Daily Aging

Simulation of a daily aging contribution is based on a daily aging rate. The daily aging value is used to generate frequency series as a linear function of time which represents the frequency change due to daily aging. Figure 8 shows a diagram of the daily aging simulation model.

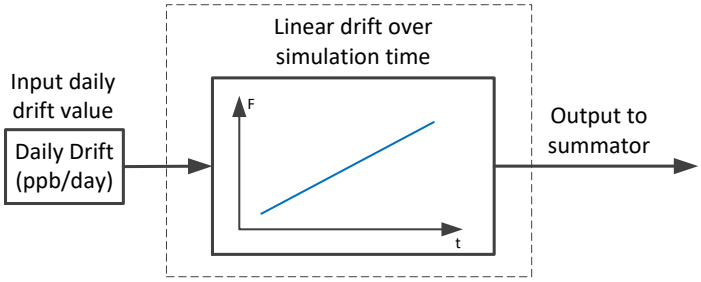

Figure 8: Daily drift (aging) simulation model